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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,043	11/16/2001	Dayna A. Byrne	01-559 1496.00174	4456

24319 7590 06/24/2004

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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/992,043	BYRNE ET AL.
	Examiner	Art Unit
	Yolanda Wilson	2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11-16-01
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Swoboda et al. (USPN 6738929B2). As per claim 1, Swoboda et al. discloses a plurality of processors; a trace circuit configured to present information at a port for debugging software in a selected processor of said processors; a connector circuit configured to couple said trace circuit to said selected processor in response to a select signal and transfer said information from said selected processor to said trace circuit while said selected processor is executing said software in column 9, lines 1-8,20-67; column 10, lines 1-23.

3. As per claim 2, Swoboda et al. discloses wherein said connector circuit is further configured to transfer data from said trace circuit to said selected processor in column 9, lines 1-8,20-67; column 10, lines 1-23.

4. As per claim 3, Swoboda et al. discloses wherein said connector circuit is further configured to transfer a first test data stream received by said selected processor to said trace circuit in column 9, lines 1-8,20-67; column 10, lines 1-23.

5. As per claim 4, Swoboda et al. discloses wherein said connector circuit is further configured to transfer a second test data stream from said trace circuit to said selected processor in column 9, lines 1-8,20-67; column 10, lines 1-23.

6. As per claim 5, Swoboda et al. discloses a first circuit configured to transfer said information from said selected processor to said trace circuit, transfer data from said trace circuit to said selected processor, and present a predetermined logic state to said processors other than said selected processor; and a second circuit configured to transfer a first test data stream received by said selected processor to said trace circuit, transfer a second test data stream from said trace circuit to said selected processor, and present a second predetermined logic state to said processors other than said selected processor in column 9, lines 1-8,20-67; column 10, lines 1-23.

7. As per claim 6, Swoboda et al. discloses a first multiplexer configured to multiplex said information from said processors to said trace circuit in response to said select signal; and a first plurality of gates each coupled to one of said processors and configured to transfer said data while selected by said select signal and present said predetermined logic state while not selected by said select signal in column 9, line 20 – column 10, line 23.

8. As per claim 7, Swoboda et al. discloses a second multiplexer configured to multiplex a plurality of first test data streams received by said processors to

said trace circuit in response to said select signal; and a second plurality of gates each coupled to one of said processors and configured to transfer a second test data stream while selected by said select signal and present said second predetermined logic state while not selected by said select signal in column 9, line 20 – column 10, line 23.

9. As per claim 8, Swoboda et al. discloses each of said gates comprises a logical AND gate having at least one input configured to receive said select signal in column 9, line 20 – column 10, line 23.

10. As per claims 9 and 19, Swoboda et al. discloses coupling a trace circuit to said selected processor in response to a select signal; transferring said information from said selected processor to said trace circuit while said selected processor is executing said software; and presenting said information received by said trace circuit at a port in column 9, lines 1-8,20-67; column 10, lines 1-23.

11. As per claim 10, Swoboda et al. discloses transferring data from said trace circuit to said selected processor in column 9, lines 1-8,20-67; column 10, lines 1-23.

12. As per claim 11, Swoboda et al. discloses transferring a first test data stream received by said selected processor to said trace circuit in column 9, lines 1-8,20-67; column 10, lines 1-23.

13. As per claim 12, Swoboda et al. discloses transferring a second test data stream from said trace circuit to said selected processor in column 9, lines 1-8,20-67; column 10, lines 1-23.

14. As per claim 13, Swoboda et al. discloses presenting a predetermined logic state to said processors other than said selected processor in response to transferring said data in column 9, lines 1-8,20-67; column 10, lines 1-23.

15. As per claim 14, Swoboda et al. discloses presenting a second predetermined logic state to said processors other than said selected processor in response to transferring said second test data stream in column 9, lines 1-8,20-67; column 10, lines 1-23.

16. As per claim 15, Swoboda et al. discloses transferring said information comprises the sub-step of multiplexing said information in response to said select signal in column 9, line 20 – column 10, line 23.

17. As per claim 16, Swoboda et al. discloses transferring said data comprises the sub-step of gating said data in response to said select signal in column 9, line 20 – column 10, line 23.

18. As per claim 17, Swoboda et al. discloses transferring said first test data stream comprises the sub-step of multiplexing said first test data stream in response to said select signal in column 9, line 20 – column 10, line 23.

19. As per claim 18, Swoboda et al. discloses transferring said second test data stream comprises the sub-step of gating said second test data stream in response to said select signal in column 9, line 20 – column 10, line 23.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SCOTT BADERMAN
PRIMARY EXAMINER